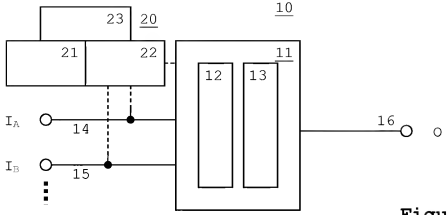

Figure 1

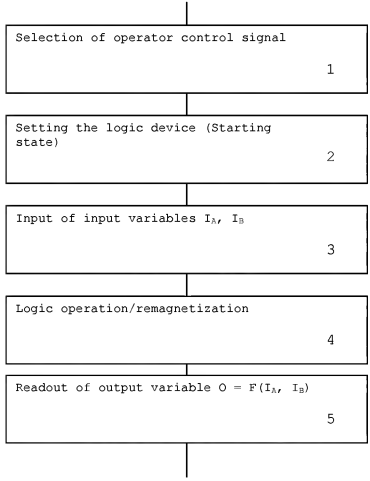

Figure 2

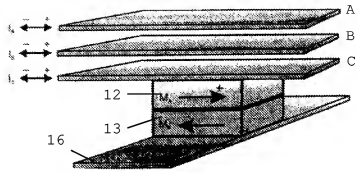

Figure 3

SET sequence for Output state	input A -I (0) input B -I (0)	input A -I (0) input B +I (1)	input A +I (1) input B -I (0)	input A +I (1) input B +I (1)	Logic table	
A,B,C=+I A,B=+I	R = high (0)	R = low (1)	R = low (1)	R = low (1)	A B out 0 0 0 1 0 1 0 1 1 1 1 1	OR
A,B,C=+I A,B=-I	R = high (0)	R = high (0)	R = high (0)	R = low (1)	A B out 0 0 0 1 0 0 0 1 0 1 1 1	AND
A,B,C=-I A,B=+I	R = low (1)	R = high (0)	R = high (0)	R = high (0)	A B out 0 0 1 1 0 0 0 1 0 1 1 0	NOR
A,B,C=-I A,B=-I	R = low (1)	R = low (1)	R = low (1)	R = high (0)	A B out 0 0 1 1 0 1 0 1 1 1 1 0	NAND

Figure 4

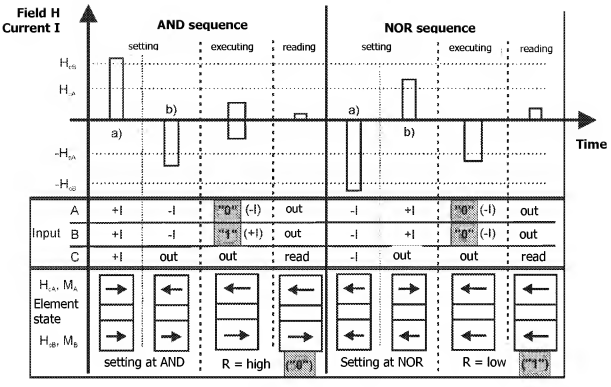

Figure 5

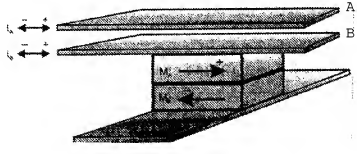

Figure 6

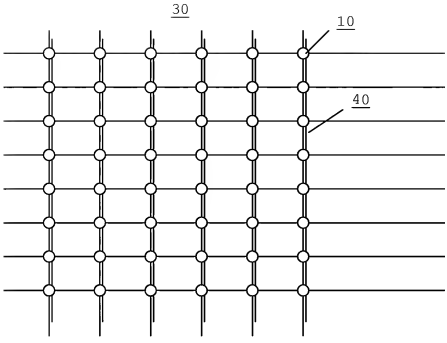

Figure 7

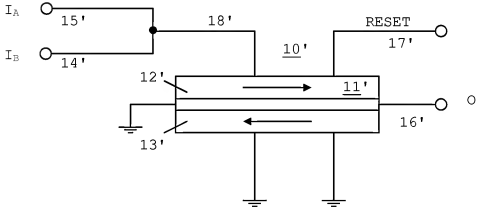

Figure 8
(state of the art)